

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Om P. Agrawal and Jinghui Zhu
Assignee: Lattice Semiconductor Corporation
Title: Block-Oriented Architecture For A Programmable Interconnect Circuit
Patent No.: 7,154,298 Date of Patent: December 26, 2006
Serial No.: 10/022,464 Filing Date: December 14, 2001
Examiner: Vibol Tan Group Art Unit: 2819
Docket No.: M-9642 US Confirmation No.: 1715

Irvine, California
November 8, 2007

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION
APPLICANT'S MISTAKE

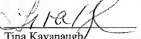
Dear Sir:

The Patentee submits herewith PTO Form 1050 Certificate of Correction. This submission deletes an error that occurred in good faith. Accordingly, the patentee requests a Certificate of Correction or an otherwise corrected patent at the expense of the Patentee to correct this omission in the specification. No new matter has been added. Please charge Deposit Account 50-2257 for the required fees.

If any questions remain or anything additional is required to correct this patent copy, please contact the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being transmitted via EFS Web to the Commission for Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.


Tina Kavanaugh

November 8, 2007

Respectfully submitted,



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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : 7,154,298 B1
ISSUE DATE : December 26, 2006
INVENTOR(S) : Om P. Agrawal and Jinghui Zhu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 15; Col. 10, line 18 - Delete "its".

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TRIM LINE

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